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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 2269-3815.1 (98-0670.00/US)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EV962541093US

Date of Deposit with USPS: December 29, 2006

Person making Deposit: Di Sanders

Application Number	Filed
09/483,712	January 14, 2000

First Named Inventor: Jiang et al.

Art Unit	Examiner
2815	M. Warren

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [ ] attorney or agent of record. Registration number _____.
- [X] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 56,957

Signature

J. Jeffrey Gunn
Typed or printed name

(801) 532-1922
Telephone number

December 29, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[X] *Total of 1 forms are submitted.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jiang et al.

Serial No.: 09/483,712

Filed: January 14, 2000

For: INTERMEDIATE STRUCTURES FOR CHIP-SCALE PACKAGES HAVING CARRIER BONDS (as amended)

Confirmation No.: 8743

Examiner: M. Warren

Group Art Unit: 2815

Attorney Docket No.: 2269-3815.1US
(98-0670.00/US)

NOTICE OF EXPRESS MAILING

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REMARKS ACCOMPANYING PRE-APPEAL BRIEF REQUEST FOR REVIEW

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

These remarks are submitted pursuant to the U.S. Patent and Trademark Office OG Notices of 12 July 2005 regarding the Pre-Appeal Brief Pilot Program. Applicant respectfully submits that the outstanding rejections of record clearly are not proper because the Examiner has failed to identify a motivation to combine the teachings of the prior art references relied upon by the Examiner, which is an essential element required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a).

BRIEF SUMMARY OF THE CLAIMS AND OUTSTANDING REJECTIONS

Claims 1 through 16 and 19 are currently pending in the present application. Claims 1 and 2 are independent, and each is directed to an intermediate structure formed during fabrication of a so-called "chip-scale package," which is a type of semiconductor device. A relatively detailed description of conventional chip-scale packages may be found in the "Background of the Invention" section of the patent application for the present invention. Claims 3 through 16 and 19 each depend directly or indirectly from independent claim 2. The outstanding rejections of record (which were first made in a final Office Action mailed October 12, 2005 and maintained in both a non-final Office Action mailed March 21, 2006 and a final Office Action mailed September 6, 2006) are as follows:

1. Claims 1, 2, 5 through 9, 13 through 16, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,677,566 to King et al. (referred to hereinafter as "King et al.") in view of U.S. Patent Application Publication No. 2001/0011773 A1 to Havens et al. (referred to hereinafter as "Havens et al."); and

2. Claims 3, 4, and 10 through 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over King et al. in view of Havens et al., and further in view of U.S. Patent No. 5,894,107 to Lee et al. (referred to hereinafter as "Lee et al.").

REMARKS

Applicants respectfully assert that there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of Havens et al. with the teachings of King et al. in the manner proposed by the Examiner. Therefore, the outstanding rejections of record are clearly improper and should not be maintained.

Applicants have admitted at Page 7 of the Response filed November 6, 2006 that King et al. teaches a final chip-scale package substantially similar to the final chip-scale package taught in the application for the present invention. Applicants and the Examiner appear to agree, however, that King et al. does not describe, teach, or suggest a method of fabricating the chip-scale package in a manner that would provide an intermediate structure as recited in either independent claim 1 or independent claim 2.

Explaining further, King et al. teaches a method of fabricating a semiconductor package 10 with reference to Figures 6-8. *King et al.*, column 4, lines 13-65. The method involves encapsulating conductive leads 12 with encapsulant material 26 and forming openings 30 in the encapsulating material 26 to expose the conductive leads 12 at electrode bond area 34 to provide an intermediate structure as shown in Figure 7. *Id.*, column 4, lines 36-40. The intermediate structure shown in Figure 7 of King et al. does not include "at least one carrier bond [attached to or disposed on] the upper surface of [a] conductive lead frame member," as recited in independent claims 1 and 2. Furthermore, the intermediate structure shown in Figure 7 is not "free of an encapsulant material to be subsequently applied to the intermediate structure," as also recited in independent claims 1 and 2. In contrast, the intermediate structure shown in Figure 7 of King et al. does not yet include any carrier bonds, but includes the encapsulating material 26. The external electrodes 28 (solder balls) are formed on the conductive leads 12 after forming the encapsulating material 26, as shown in Figure 8. *King et al.*, column 4, lines 36-51.

In an effort to satisfy the deficiency, the Examiner has relied upon Havens et al. Havens et al. teaches a hydrophobic hermetic covering that can be applied to substantially all external surfaces of an electronic package, and methods of applying the hydrophobic hermetic covering to external surfaces of an electronic package. Havens et al. teaches that the hermetic covering may comprise a thin layer (e.g., 0.001 inches) of Teflon® material or other fluorinated thermoset material. *Havens et al.*, Page 3, Paragraphs [0031], [0033], [0037]. Havens et al. further teaches that the hydrophobic hermetic covering can be applied to an electronic package either before (*See e.g., Id.*, Page 2, Paragraph [0028] – Page 3, Paragraph [0031]) or after (*See Id.*, Page 5, Paragraphs [0057]-[0058]) attaching carrier bonds (e.g., solder balls 6) to a substrate 3 of an electronic package 1 to which the hydrophobic hermetic covering is applied.

As discussed at Pages 7-8 of the Response filed November 6, 2006, Applicants admit that one of ordinary skill in the art, considering the combined teachings of King et al. and Havens et al. as a whole at the time the present invention was made (as required by the Manual of Patent Examining Procedure (MPEP) § 2141(II)) may have been motivated to replace the encapsulating material 26 of the device taught by King et al. (*See e.g., King et al.*, column 3, lines 28-33) with a hermetic covering as taught in Havens et al. to address the moisture sensitivity problem addressed by Havens et al. (*See e.g., Havens et al.*, Page 2, Paragraph [0025]). Applicants

respectfully assert, however, that in doing so, one of ordinary skill in the art clearly would have been motivated to apply the hermetic covering *before* attaching the carrier bonds to the conductive leads of the device taught by King et al., and not after.

King et al. teaches applying the encapsulating material before attaching the carrier bonds (external electrodes 28). Havens et al. also teaches that the hermetic covering can be applied before attaching the carrier bonds (solder balls 6). As a result, this method would be in accordance with both the teachings of King et al. and Havens et al., would require less modifications of the teachings of King et al. to incorporate the hermetic covering taught by Havens et al., and as such, clearly would have been the obvious method of choice to one of ordinary skill in the art at the time the present invention was made. While Havens et al. teaches that the hermetic covering may be applied either before or after attaching the carrier bonds 6 to the electronic package 1, there is no reason one of ordinary skill in the art would be motivated to unnecessarily further modify the teachings of King et al. so as to attach the carrier bonds before applying the hermetic covering. In other words, the prior art references do not teach or suggest the desirability of attaching the carrier bonds before applying the hermetic covering as opposed to attaching the carrier bonds after applying the hermetic covering, and to do so would require unnecessary further modifications to the teachings of King et al.

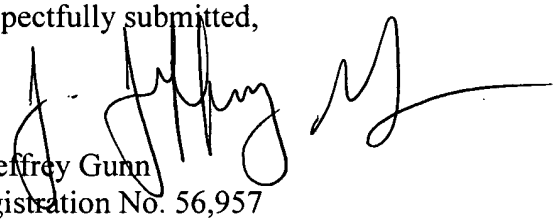
The Examiner has asserted at Pages 6-7 of the Office Action mailed September 6, 2006, that "[a]t the very least Havens discloses [0026] that in one embodiment, all of the package, including all external conductor surfaces, are covered (e.g., to facilitate shipment)," and that as a result, "[o]ne of ordinary skill in the art would be motivated to improve King by using the inventive structure of Havens to improve the reliability and product yield or facilitate shipment." Applicants respectfully assert that there is no evidence that methods in which the carrier bonds are attached prior to applying the hermetic covering taught by Havens et al. would result in higher reliability and product yield than methods in which the carrier bonds are attached after applying the hermetic covering. Furthermore, Applicants respectfully assert that one of ordinary skill in the art would recognize that, in methods in which the hermetic covering taught by Havens et al. is applied prior to attaching the carrier bonds, the electronic package could be shipped prior to attaching the carrier bonds, in which case all of the package, including all of the external

surfaces, would be covered by the hermetic covering, thereby facilitating shipment in the manner taught by Havens et al.

In sum, there is no teaching or suggestion in the cited prior art references that any benefit would be achieved by attaching the carrier bonds to the conductive leads of the device taught by King et al. prior to applying the hermetic covering taught by Havens et al. In other words, the prior art references do not teach or suggest any desirability for attaching the carrier bonds to the conductive leads before applying the hermetic covering instead of after applying the hermetic covering. In contrast, however, applying the hermetic covering taught by Havens et al. prior to attaching the carrier bonds to the conductive leads of the device taught by King et al. accords with the teachings of both Havens et al. and King et al. and would require fewer modifications to the teachings of King et al. Therefore, one of ordinary skill in the art, considering the teachings of King et al. and Havens et al. in combination and as a whole at the time the present invention was made, clearly would have been motivated to apply the hermetic covering taught by Havens et al. to the device taught by King et al. before attaching the carrier bonds to the leads of the device.

As there is clearly no motivation or suggestion to combine the teachings of the prior art references in the manner proposed by the Examiner, which is an essential element required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), the outstanding rejections of record are clearly improper and should not be maintained on appeal.

Respectfully submitted,



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